REMARKS

Claims 1, 2, 3, 4, 5, 6, and 12-16 stand objected to. The abstract stands objected to because the title is included. Claims 1-16 stands rejected under 35 USC §102(e) as being anticipated by Sani et al., U.S. patent 6,794,914

Claims 1, 2, 3, 4, 5, 6, 7, 8, and 11-16 have been amended to more clearly state the invention and to overcome the objections to claims1, 2, 3, 4, 5, 6, and 12-16. Reconsideration and withdrawal of the objections to claims1, 2, 3, 4, 5, 6, and 12-16 is respectfully requested. Reconsideration and allowance of each of the pending claims 1-16, as amended, is respectfully requested.

Sani et al., U.S. patent 6,794,914 discloses an integrated circuit including a Multi-Threshold CMOS (MTCMOS) latch combining low voltage threshold CMOS circuits with high voltage threshold CMOS circuits. The low voltage threshold circuits include a majority of the circuits in the signal path of the latch to ensure high performance of the latch. The latch further includes high voltage threshold circuits to eliminate leakage paths from the low voltage threshold circuits when the latch is in a sleep mode. A single-phase latch and a two-phase latch are provided. Each of the latches is implemented with master and slave registers. Data is held in either the master register or the slave register depending on the phase or phases of the clock signals. A multiplexer may alternatively be implemented prior to the master latch for controlling an input signal path during sleep and active modes of the latch and for providing a second input signal path for test. At column 6, lines 53-67 states: Thus, it may be appreciated that embodiments of the MTCMOS latch 200 configuration may

have low threshold voltage circuits in only the signal path and may have high threshold voltage circuits in the feedback and non-critical paths of the latch. For example, in FIG. 2, the feedback inverters, 230 and 260, may be implemented entirely as high threshold voltage circuits while the inverters in the direct signal path, 220 and 250, as well as the transmission gates, 210 and 240, may be implemented using low threshold voltage circuits. Alternatively, some of the circuits in the direct signal path may be low threshold voltage circuits while others are high threshold voltage circuits. The high threshold voltage circuits may be placed such that they provide a low current leakage path for the low threshold voltage circuits.

As amended, each of the independent claims 1 and 11 recite the steps of identifying logic blocks in critical data and data clock paths of a L1 latch and a L2 latch of a LSSD latch; substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor used in said identified logic blocks in the critical data and data clock paths of said L1 latch and said L2 latch of said LSSD latch; and selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only with RVT transistors, or low leakage (LLD) transistors.

Independent claim 7, as amended, recites a level sensitive scan design (LSSD) latch for implementing enhanced performance with reduced quiescent power dissipation comprising: critical data and data clock paths of a L1 latch and a L2 latch of the LSSD latch; non-critical sections of said L1 latch and said L2 latch of the LSSD latch; a low voltage threshold (LVT) transistor being used only in said critical data and

data clock paths and implementing each transistor in said critical data and data clock paths of said L1 latch and said L2 latch of the LSSD latch; and said non-critical sections being implemented only with regular voltage threshold (RVT) transistors, or low leakage (LLD) transistors.

Applicants respectfully submit that each of the independent claims 1, 7, and 11, as amended, are patentable over the references of record including Sani et al. The recited steps of the invention of substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor used in said identified logic blocks in the critical data and data clock paths of said L1 latch and said L2 latch of said LSSD latch; and selectively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only with RVT transistors, or low leakage (LLD) transistors, are only taught and claimed by applicants. Sani et al. provides no suggestion for substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor used in said identified logic blocks in the critical data and data clock paths of said L1 latch and said L2 latch of said LSSD latch. Sani et al. provides no suggestion for electively implementing non-critical sections of said L1 latch and said L2 latch of said LSSD latch including scan input and scan clock paths only with RVT transistors, or low leakage (LLD) transistors. Thus, each of the independent claims 1, and 11, as amended, is patentable.

Further only Applicants teach a low voltage threshold (LVT) transistor being used only in said critical data and data clock paths and implementing each

transistor in said critical data and data clock paths of said L1 latch and said L2 latch of the LSSD latch; and said non-critical sections being implemented only with regular voltage threshold (RVT) transistors, or low leakage (LLD) transistors, as taught and claimed in independent claim 7, as amended. Sani et al. provides no suggestion of a LSSD latch including these features. Thus, independent claim 7, as amended, is patentable.

Dependent claims 2-6, 8-10, and 12-16 further define the invention depending from respective patentable claims 1, 7, and 11, as amended, and are likewise patentable.

Applicants have reviewed all the art of record, and respectfully submit that the claimed invention is patentable over all the art of record, including the references not relied upon by the Examiner for the rejection of the pending claims.

It is believed that the present application is now in condition for allowance and allowance of each of the pending claims 1-16, as amended, is respectfully requested. Prompt and favorable reconsideration is respectfully requested.

If the Examiner upon considering this amendment should find that a telephone interview would be helpful in expediting allowance of the present application, the Examiner is respectfully urged to call the applicants' attorney at the number listed below.

Respectfully submitted,

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